

**PATENT NUMBER**

**O.J.P.E.**

**PATENT DATE**

SCANNED Ed 1 O.A. TM

APPLICATION NO. 09/997071	CONT/PRIOR	CLASS 430	SUBCLASS 3.11	ART UNIT 1756	EXAMINER S. J. ... T. J. ...
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Process for inhibiting edge peeling of coating on semiconductor substrate during formation of integrated circuit structure thereon

PTC-2040  
12/99

**ORIGINAL**

**CROSS REFERENCE(S)**

**CLASS**

SUBCLASS

## CLASS

**SUBCLASS (ONE SUBCLASS PER BLOCK)**

### INTERNATIONAL CLASSIFICATION

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>	
			<b>ISSUE FEE</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____  _____  _____	_____ (Primary Examiner) (Date)			
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		<b>ISSUE BATCH NUMBER</b>	
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